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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/826,612	SHIBATA ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *8-11 and 21-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,12-20 and 25-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's Amendment filed 01/19/2006 has been reviewed and placed of record in the file.

2. Applicant's arguments with respect to amended claims 1-24 and new claims 25-30, filed 01/19/2006, have been considered but they are moot in view of new ground(s) of rejection.

Election/Restrictions

3. Claims 8-11 and 21-24 are still withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being still no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 08/29/2005 and 01/19/2006.

4. This application contains claims 8-11 and 21-24 drawn to an invention nonelected with traverse in the reply filed on 08/29/2005 and 01/19/2006, as noted above. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action, including amendment to their respective independent claims so as their respective independent claims are in condition for allowance (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. **Claims 1-7, 12-20, and 25-30** are rejected under 35 U.S.C. §103(a) as being unpatentable over Chan U.S. Patent Application Publication 20030005214 (the '214 reference, cited in a previous office action) in view of Sakagami et al. U.S. Patent 5,838,041 (the '041 reference).

Chan in the '214 reference discloses a semiconductor memory device in the background art comprising a nonvolatile memory section and a volatile memory section, but fails to teach limitations as claimed for a nonvolatile memory cell for the nonvolatile memory section.

Referring to **claim 1**, the '214 reference discloses a semiconductor memory device comprising:

a nonvolatile memory section (the Flash memory section of the Flash/SRAM package, paragraphs [0004] to [0006], particularly paragraph [0006]); and

a volatile memory section (the SRAM memory section of the Flash/SRAM package, paragraphs [0004] to [0006], particularly paragraph [0006]), wherein

the nonvolatile memory section includes a nonvolatile memory cell.

However, the reference does not teach that the nonvolatile memory cell includes charge storage areas on both side of a gate electrode of the cell. Specifically, the reference does not teach that the nonvolatile memory cell having a single gate electrode formed on a semiconductor layer via a gate insulating film, a channel region disposed under the single gate electrode, diffusion regions disposed on both sides of the channel region and having a conductive type opposite to that of the channel region, and memory functional units formed on both sides of the single gate electrode and having a function for retaining charges.

Sakagami in the '041 reference, in disclosing a semiconductor memory device, teaches in the first embodiment – Fig. 2 - that a nonvolatile memory cell includes charge storage areas (19, 19) on both side of a single gate electrode (13) of the cell so as to form highly reliable memory cells with reduced sizes (paragraph bridging columns 2 and 3). Specifically, the '041 reference teaches a nonvolatile memory cell having a gate electrode (13, Fig. 2) formed on a semiconductor layer (1) via a gate insulating film (11), a channel region (no number) disposed under the gate electrode, diffusion regions (20, 21) disposed on both sides of the channel region and having a conductive type opposite to that of the channel region, and memory functional units (19, 19) formed on both sides of the gate electrode and having a function for retaining charges (column 4, lines 5-35) so as to form highly reliable memory cells with reduced sizes (paragraph bridging columns 2 and 3, col. 3, lines 5-15).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a prior art semiconductor memory device, such as one disclosed by the 214 reference, such that a nonvolatile memory cell of the nonvolatile memory section includes charge storage areas on both side of a single gate of the cell. One would have been motivated to make such a change in view of the teachings in Sakagami that such a change results in highly reliable memory cells with reduced sizes, as detailed above.

Referring to **claim 12**, the '214 reference discloses a semiconductor device comprising:

a semiconductor memory device that comprises:

a nonvolatile memory section (the Flash memory section of the Flash/SRAM package, paragraphs [0004] to [0006], particularly paragraph [0006]);

a volatile memory section (the SRAM memory section of the Flash/SRAM package, paragraphs [0004] to [0006], particularly paragraph [0006]), wherein

the nonvolatile memory section includes a nonvolatile memory cell; and

a logical operation section (such as section 22, Fig. 2, or section 24, Fig. 4) for performing operation processing on the basis of information stored in the semiconductor memory device.

However, the reference does not teach that the nonvolatile memory cell includes charge storage areas on both side of a gate electrode of the cell. Specifically, the reference does not teach that the nonvolatile memory cell having a single gate electrode formed on a semiconductor layer via a gate insulating film, a channel region disposed under the single gate electrode, diffusion regions disposed on both sides of the channel region and having a conductive type opposite to that of the channel region, and memory functional units formed on both sides of the single gate electrode and having a function for retaining charges.

Sakagami in the '041 reference, in disclosing a semiconductor memory device, teaches in the first embodiment – Fig. 2 - that a nonvolatile memory cell includes charge storage areas (19, 19) on both side of a single gate electrode (13) of the cell so as to form highly reliable memory cells with reduced sizes (paragraph bridging columns 2 and 3). Specifically, the '041 reference teaches a nonvolatile memory cell having a gate electrode (13, Fig. 2) formed on a semiconductor layer (1) via a gate insulating film (11), a channel region (no number) disposed under the gate electrode, diffusion regions (20, 21) disposed on both sides of the channel region and having a conductive type opposite to that of the channel region, and memory functional units (19, 19) formed on both sides of the gate electrode and having a function for retaining charges

(column 4, lines 5-35) so as to form highly reliable memory cells with reduced sizes (paragraph bridging columns 2 and 3, col. 3, lines 5-15).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a prior art semiconductor memory device, such as one disclosed by the 214 reference, such that a nonvolatile memory cell of the nonvolatile memory section includes charge storage areas on both side of a single gate of the cell. One would have been motivated to make such a change in view of the teachings in Sakagami that such a change results in highly reliable memory cells with reduced sizes, as detailed above.

Referring to **claims 13 and 14**, similarly as detailed above for claims 1 and 12, the '214 reference discloses s portable electronic apparatus (paragraph [0008], the first few lines particularly) as claimed and the '041 reference teaches the advantage of the nonvolatile memory cell including charge storage areas on both side of a single gate of the cell.

Referring to **claims 2 and 15**, the '214 reference further discloses that the volatile memory section includes an SRAM, as noted above.

Referring to **claims 3 and 16**, the '214 reference further discloses that the nonvolatile memory cell and the volatile memory cell (a memory cell of the SRAM portion) are formed on a single chip ("same package module", paragraph [0006], "chip" is interpreted broadly), as noted above.

Referring to **claims 6 and 19**, the '214 reference further discloses, as noted above, that:

a first chip forming the nonvolatile memory section;

a second chip forming the volatile memory section; and

a single package containing therein the first chip and the second chip (paragraph [0006]).

Referring to **claims 4 and 17**, the '214 reference further discloses that the volatile memory section (as is known in the art) could include a DRAM (paragraph [0004]).

Referring to **claims 5 and 18**, although both the references do not disclose a refreshing operation means for refreshing the DRAM, a refreshing operation means for refreshing the DRAM is required for the DRAM to function, as is known in the DRAM art.

Referring to **claims 7 and 20**, the '554 reference further teaches that at least a part of the memory functional units (19, Fig. 2) overlaps with a part of the diffusion region (20, 21).

Referring to **claims 25-28**, although both the references do not disclose in details a structure of a memory cell of the volatile memory section (the SRAM part of the Flash/SRAM package), it is known that a SRAM cell at the time the invention was made comprises a transistor having a gate electrode, a gate insulating film, a channel region disposed under the gate electrode and diffusion regions (also known as source/drain regions) disposed on both sides of the channel region. In other words, at the time the invention was made, it is reasonable to conclude that said volatile memory section, which comprised a transistor, had substantially the same structure as the nonvolatile memory section, which also comprised a transistor as detailed above, as recited in the claims.

However, both the references do not disclose that said volatile memory section has additional extension regions (otherwise known as lightly doped drain regions – or LDD – and in reference to claims 27-28) adjacent to the diffusion regions (also known as source/drain regions) on both sides of the channel region.

Nevertheless, because Applicant has not disclosed in the specification as to any advantage for adding the additional extension regions, the adding of the additional extension

regions to the diffusion regions are considered obvious design choices and are not patentable since no unobvious or unexpected results are obtained from these changes.

Referring to **claims 29-30**, the '041 reference further discloses that wherein each memory functional unit (19, which comprises layers 14, 17, 18) is a film having a function of trapping charges, which is an insulator film (14, 17, 18) including a silicon nitride film (17), satisfying the requirement that wherein each memory functional unit is a film having a function of accumulating or trapping charges or a function of holding a charge polarized state, which is an insulator film including a silicon nitride film; an insulator film having therein a conductor film or a semiconductor layer; an insulator film having therein one or more dots made of a conductor or a semiconductor; or a single layer or a lamination layer of an insulator film including a ferroelectric film in which internal charges are polarized by an electric field and its state is held.

6. **Claims 1-7, 12-20, and 25-30** are rejected under 35 U.S.C. §103(a) as being unpatentable over Chan U.S. Patent Application Publication 20030005214 (the '214 reference, cited in a previous office action) in view of Takahashi U.S. Patent 6,642,586 (the '586 reference).

Chan in the '214 reference discloses a semiconductor memory device in the background art comprising a nonvolatile memory section and a volatile memory section, but fails to teach limitations as claimed for a nonvolatile memory cell for the nonvolatile memory section.

Referring to **claim 1**, the '214 reference discloses a semiconductor memory device comprising:

a nonvolatile memory section (the Flash memory section of the Flash/SRAM package, paragraphs [0004] to [0006], particularly paragraph [0006]); and

a volatile memory section (the SRAM memory section of the Flash/SRAM package, paragraphs [0004] to [0006], particularly paragraph [0006]), wherein

the nonvolatile memory section includes a nonvolatile memory cell.

However, the reference does not teach that the nonvolatile memory cell includes charge storage areas on both side of a gate electrode of the cell. Specifically, the reference does not teach that the nonvolatile memory cell having a single gate electrode formed on a semiconductor layer via a gate insulating film, a channel region disposed under the single gate electrode, diffusion regions disposed on both sides of the channel region and having a conductive type opposite to that of the channel region, and memory functional units formed on both sides of the single gate electrode and having a function for retaining charges.

Takahashi in the '586 reference, in disclosing a semiconductor memory device, teaches in the first embodiment – Fig. 2 - that a nonvolatile memory cell includes charge storage areas (6, 6) on both side of a single gate electrode (5) of the cell so as to provide a semiconductor device capable of storing data of two bits in one memory cell and being driven at a low voltage (paragraph bridging columns 3 and 4). Specifically, the '586 reference teaches a nonvolatile memory cell having a gate electrode (5, Fig. 2) formed on a semiconductor layer (1) via a gate insulating film (4), a channel region (no number) disposed under the gate electrode, diffusion regions (2, 2) disposed on both sides of the channel region and having a conductive type opposite to that of the channel region, and memory functional units (6, 6) formed on both sides of the gate electrode and having a function for retaining charges (col. 4, lines 3+, col. 6, lines 21+) so as to provide a semiconductor device capable of storing data of two bits in one memory cell and being driven at a low voltage (column 3, lines 65+).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a prior art semiconductor memory device, such as one disclosed by the 214 reference, such that a nonvolatile memory cell of the nonvolatile memory section includes charge storage areas on both side of a single gate of the cell. One would have been motivated to make such a change in view of the teachings in Takahashi that such a change results in a semiconductor device capable of storing data of two bits in one memory cell and being driven at a low voltage, as detailed above.

Referring to **claim 12**, the '214 reference discloses a semiconductor device comprising:

a semiconductor memory device that comprises:

a nonvolatile memory section (the Flash memory section of the Flash/SRAM package, paragraphs [0004] to [0006], particularly paragraph [0006]);

a volatile memory section (the SRAM memory section of the Flash/SRAM package, paragraphs [0004] to [0006], particularly paragraph [0006]), wherein

the nonvolatile memory section includes a nonvolatile memory cell; and

a logical operation section (such as section 22, Fig. 2, or section 24, Fig. 4) for performing operation processing on the basis of information stored in the semiconductor memory device.

However, the reference does not teach that the nonvolatile memory cell includes charge storage areas on both side of a gate electrode of the cell. Specifically, the reference does not teach that the nonvolatile memory cell having a single gate electrode formed on a semiconductor layer via a gate insulating film, a channel region disposed under the single gate electrode, diffusion regions disposed on both sides of the channel region and having a conductive type

opposite to that of the channel region, and memory functional units formed on both sides of the single gate electrode and having a function for retaining charges.

Takahashi in the '586 reference, in disclosing a semiconductor memory device, teaches in the first embodiment – Fig. 2 - that a nonvolatile memory cell includes charge storage areas (6, 6) on both side of a single gate electrode (5) of the cell so as to provide a semiconductor device capable of storing data of two bits in one memory cell and being driven at a low voltage (paragraph bridging columns 3 and 4). Specifically, the '586 reference teaches a nonvolatile memory cell having a gate electrode (5, Fig. 2) formed on a semiconductor layer (1) via a gate insulating film (4), a channel region (no number) disposed under the gate electrode, diffusion regions (2, 2) disposed on both sides of the channel region and having a conductive type opposite to that of the channel region, and memory functional units (6, 6) formed on both sides of the gate electrode and having a function for retaining charges (col. 4, lines 3+, col. 6, lines 21+) so as to provide a semiconductor device capable of storing data of two bits in one memory cell and being driven at a low voltage (column 3, lines 65+).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a prior art semiconductor memory device, such as one disclosed by the 214 reference, such that a nonvolatile memory cell of the nonvolatile memory section includes charge storage areas on both side of a single gate of the cell. One would have been motivated to make such a change in view of the teachings in Takahashi that such a change results in a semiconductor device capable of storing data of two bits in one memory cell and being driven at a low voltage, as detailed above.

Referring to **claims 13 and 14**, similarly as detailed above for claims 1 and 12, the '214 reference discloses s portable electronic apparatus (paragraph [0008], the first few lines particularly) as claimed and the '041 reference teaches the advantage of the nonvolatile memory cell including charge storage areas on both side of a single gate of the cell.

Referring to **claims 2 and 15**, the '214 reference further discloses that the volatile memory section includes an SRAM, as noted above.

Referring to **claims 3 and 16**, the '214 reference further discloses that the nonvolatile memory cell and the volatile memory cell (a memory cell of the SRAM portion) are formed on a single chip ("same package module", paragraph [0006], "chip" is interpreted broadly), as noted above.

Referring to **claims 6 and 19**, the '214 reference further discloses, as noted above, that:

a first chip forming the nonvolatile memory section;

a second chip forming the volatile memory section; and

a single package containing therein the first chip and the second chip (paragraph [0006]).

Referring to **claims 4 and 17**, the '214 reference further discloses that the volatile memory section (as is known in the art) could include a DRAM (paragraph [0004]).

Referring to **claims 5 and 18**, although both the references do not disclose a refreshing operation means for refreshing the DRAM, a refreshing operation means for refreshing the DRAM is required for the DRAM to function, as is known in the DRAM art.

Referring to **claims 7 and 20**, the '586 reference further teaches that at least a part of the memory functional units (6, Fig. 2) overlaps with a part of the diffusion region (2).

Referring to **claims 25-28**, although both the references do not disclose in details a structure of a memory cell of the volatile memory section (the SRAM part of the Flash/SRAM package), it is known that a SRAM cell at the time the invention was made comprises a transistor having a gate electrode, a gate insulating film, a channel region disposed under the gate electrode and diffusion regions (also known as source/drain regions) disposed on both sides of the channel region. In other words, at the time the invention was made, it is reasonable then to conclude that said volatile memory section, which comprised a transistor, had substantially the same structure as the nonvolatile memory section, which also comprised a transistor as detailed above, as recited in the claims.

However, both the references do not disclose that said volatile memory section has additional extension regions (otherwise known as lightly doped drain regions – or LDD – and in reference to claims 27-28) adjacent to the diffusion regions (also known as source/drain regions) on both sides of the channel region.

Nevertheless, because Applicant has not disclosed in the specification as to any advantage for adding the additional extension regions, the adding of the additional extension regions to the diffusion regions are considered obvious design choices and are not patentable since no unobvious or unexpected results are obtained from these changes.

Referring to **claims 29-30**, the '586 reference further discloses that wherein each memory functional unit (6, which comprises layers 6A, 6B, 6C) is a film having a function of trapping charges (col. 4, lines 3+), which is an insulator film (6A, 6B, 6C) including a silicon nitride film (6B), satisfying the requirement that wherein each memory functional unit is a film having a function of accumulating or trapping charges or a function of holding a charge polarized state,

which is an insulator film including a silicon nitride film; an insulator film having therein a conductor film or a semiconductor layer; an insulator film having therein one or more dots made of a conductor or a semiconductor; or a single layer or a lamination layer of an insulator film including a ferroelectric film in which internal charges are polarized by an electric field and its state is held.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office Action. See MPEP § 706.07(a).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
February 02, 2006